

Fig. 1 Block Diagram of Tree System

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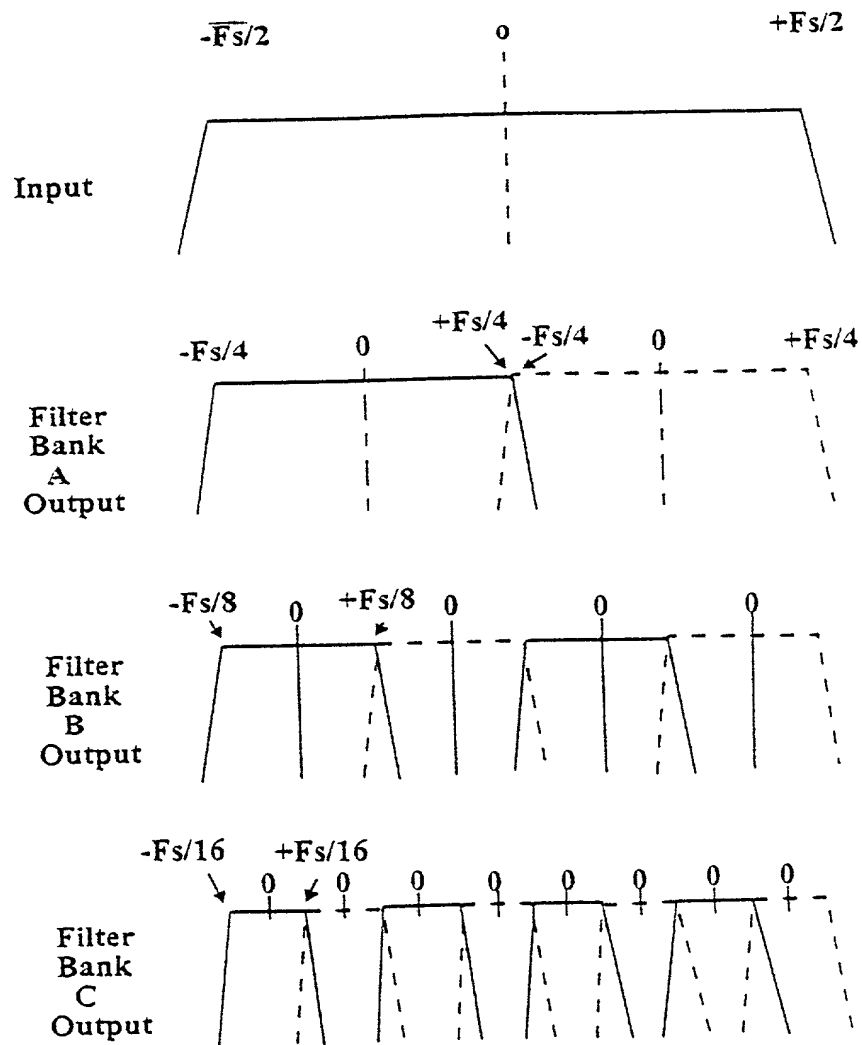


Fig. 2 Frequency Band Splitting

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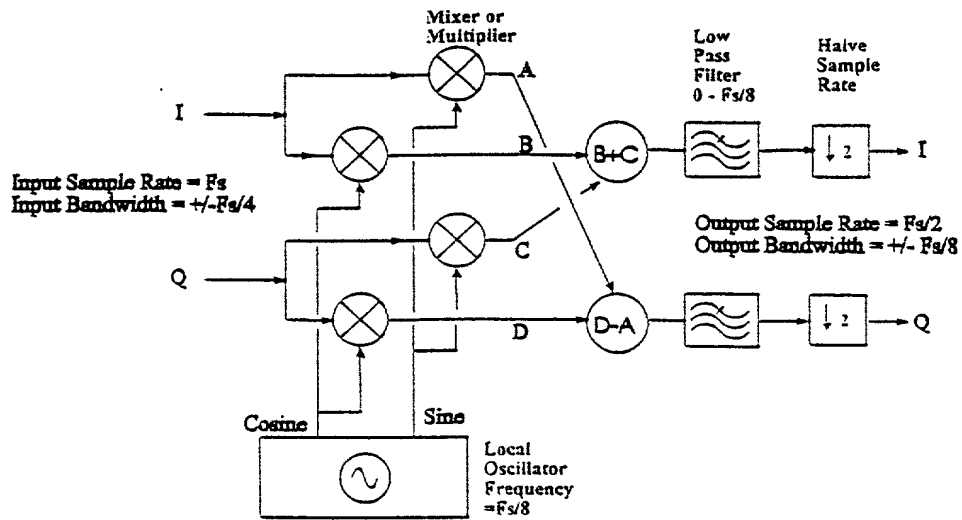


Fig. 3 Complex Down-Converter (CDC)

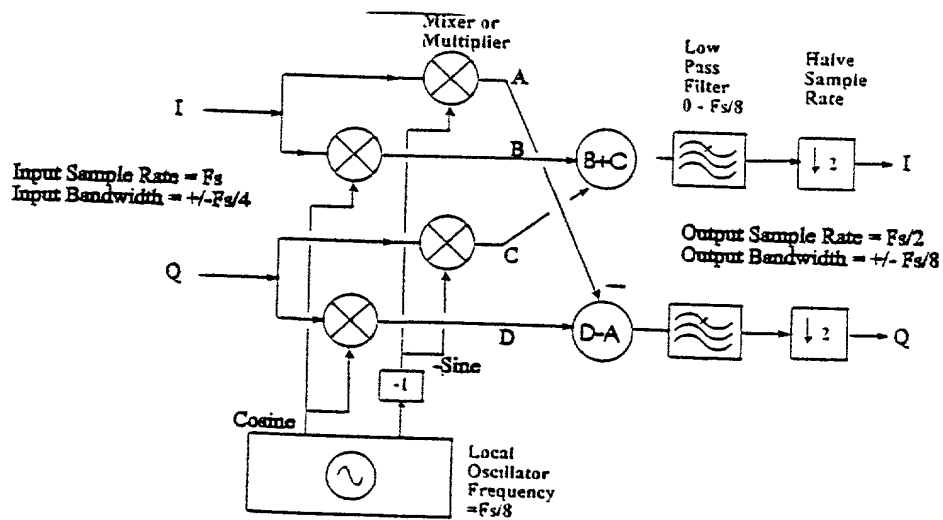


Fig. 4 Complex Up-Converter (CUC)

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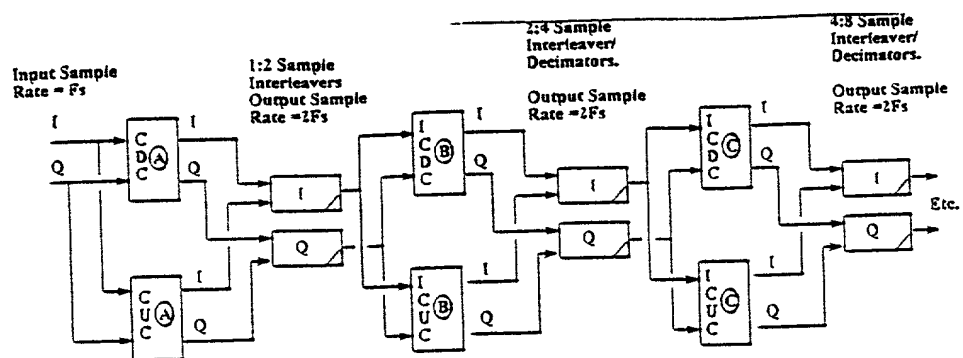


Figure 5 Block Diagram of Interleaved System

09774673, 020104

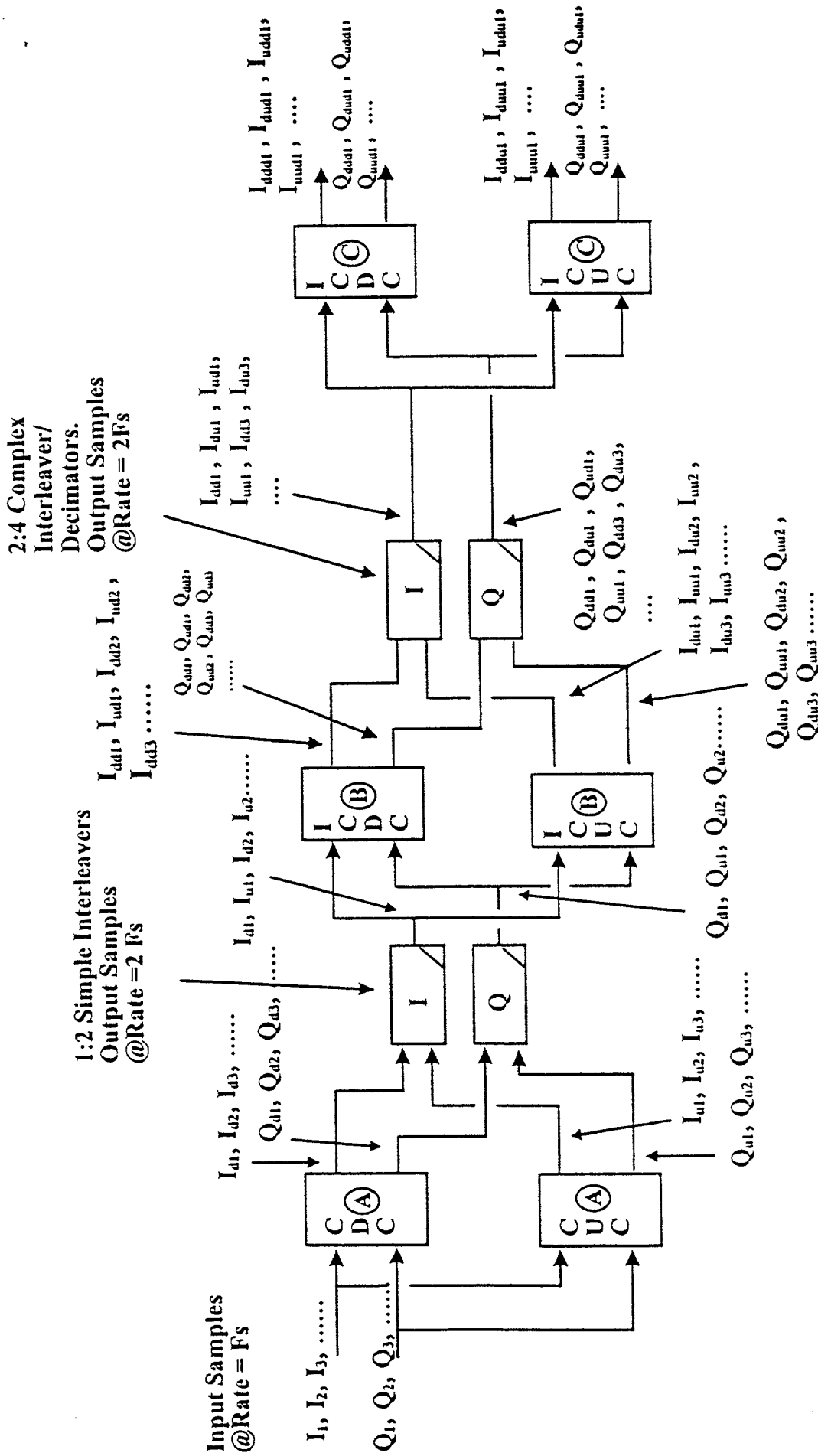


Figure 6 Detail of Interleavers

Multiplier

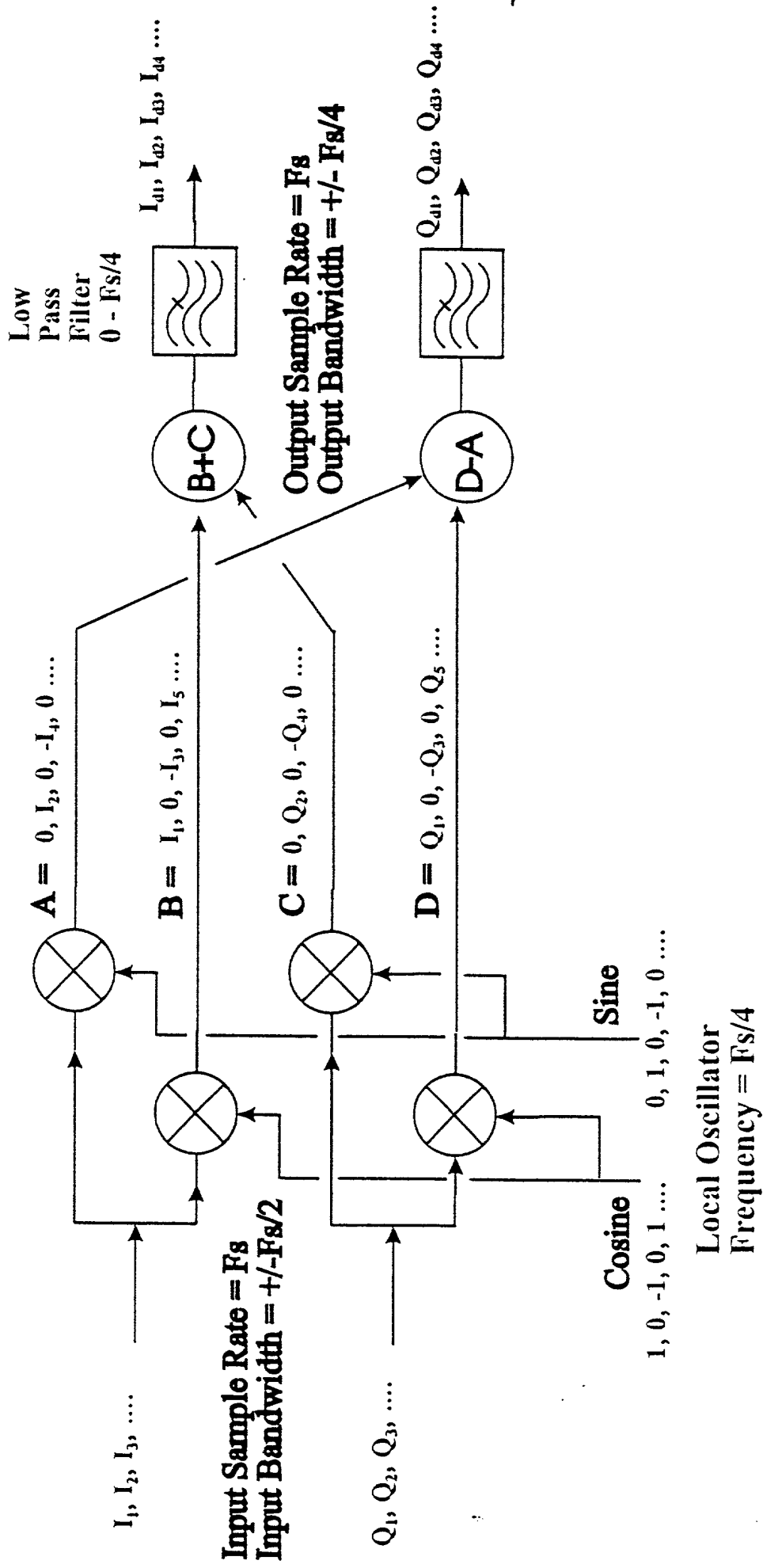


Fig. 7 BASIC CDC(A) ARCHITECTURE

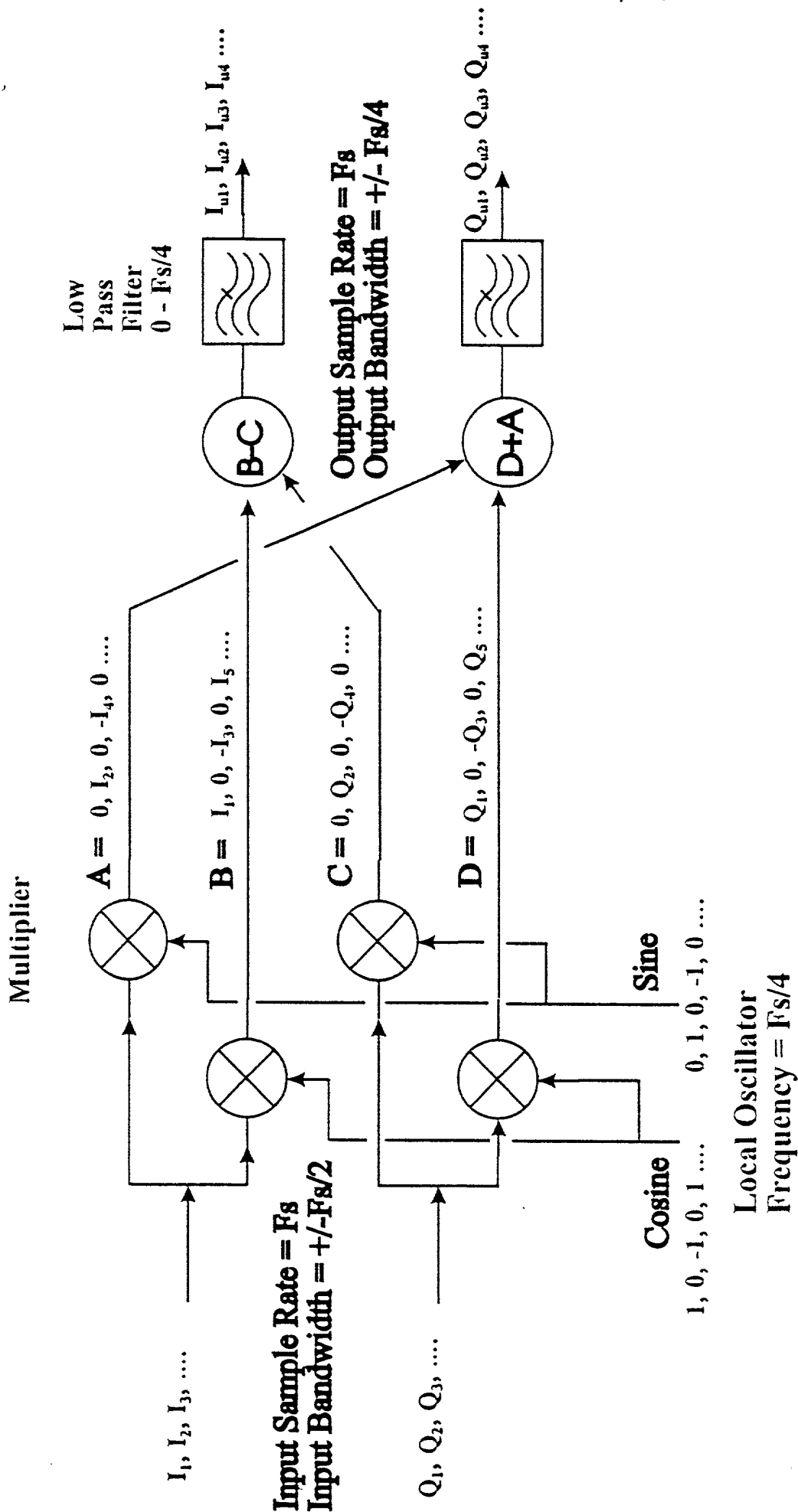


Fig. 3 BASIC CUC(A) ARCHITECTURE

Input Sample Rate = $F_s/2$
 Input Bandwidth = $\pm F_s/2$

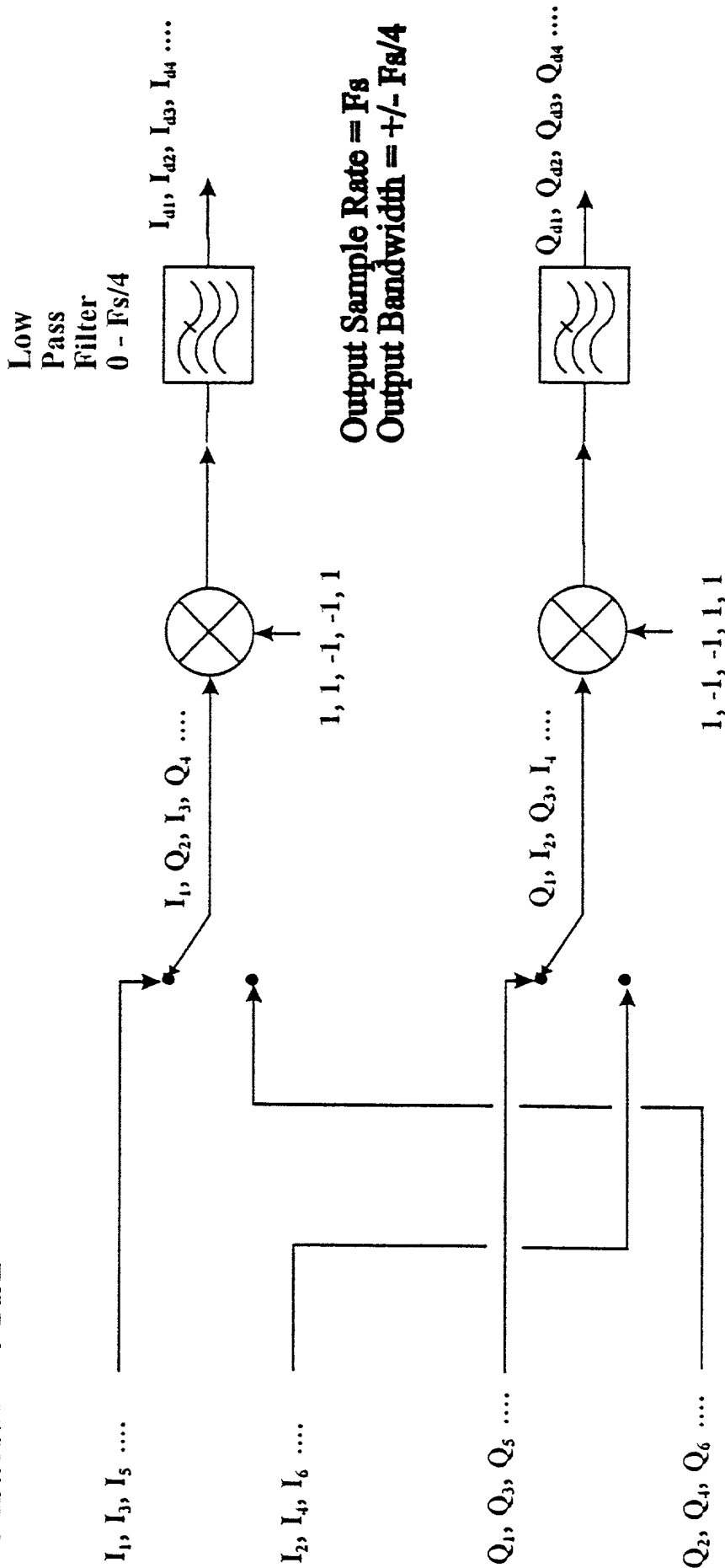


Fig. 9 MODIFIED CDC(A) ARCHITECTURE

Input Sample Rate = $F_s/2$
Input Bandwidth = $\pm F_s/2$

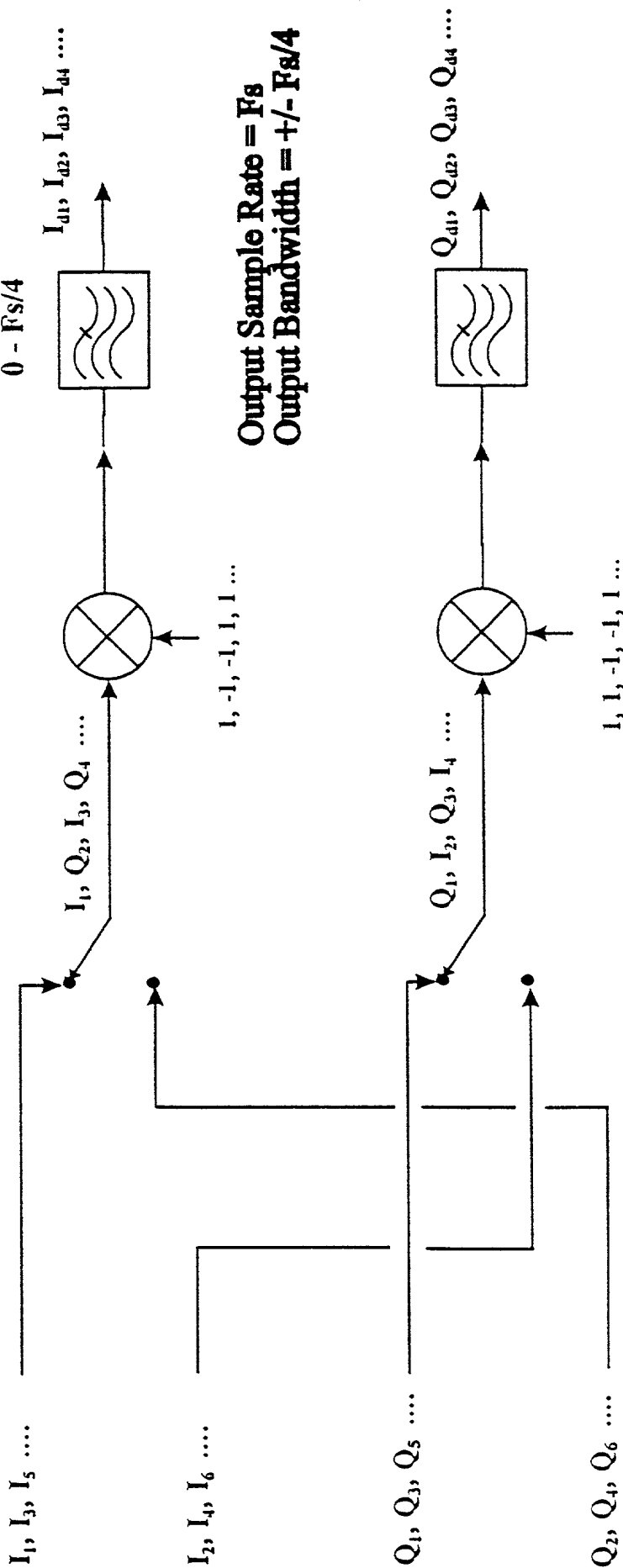


Fig. 10 MODIFIED CUC(A) ARCHITECTURE

Low
Pass
Filter
 $0 - F_s/4$

Input Sample Rate = $F_s/2$
Input Bandwidth = $\pm F_s/2$

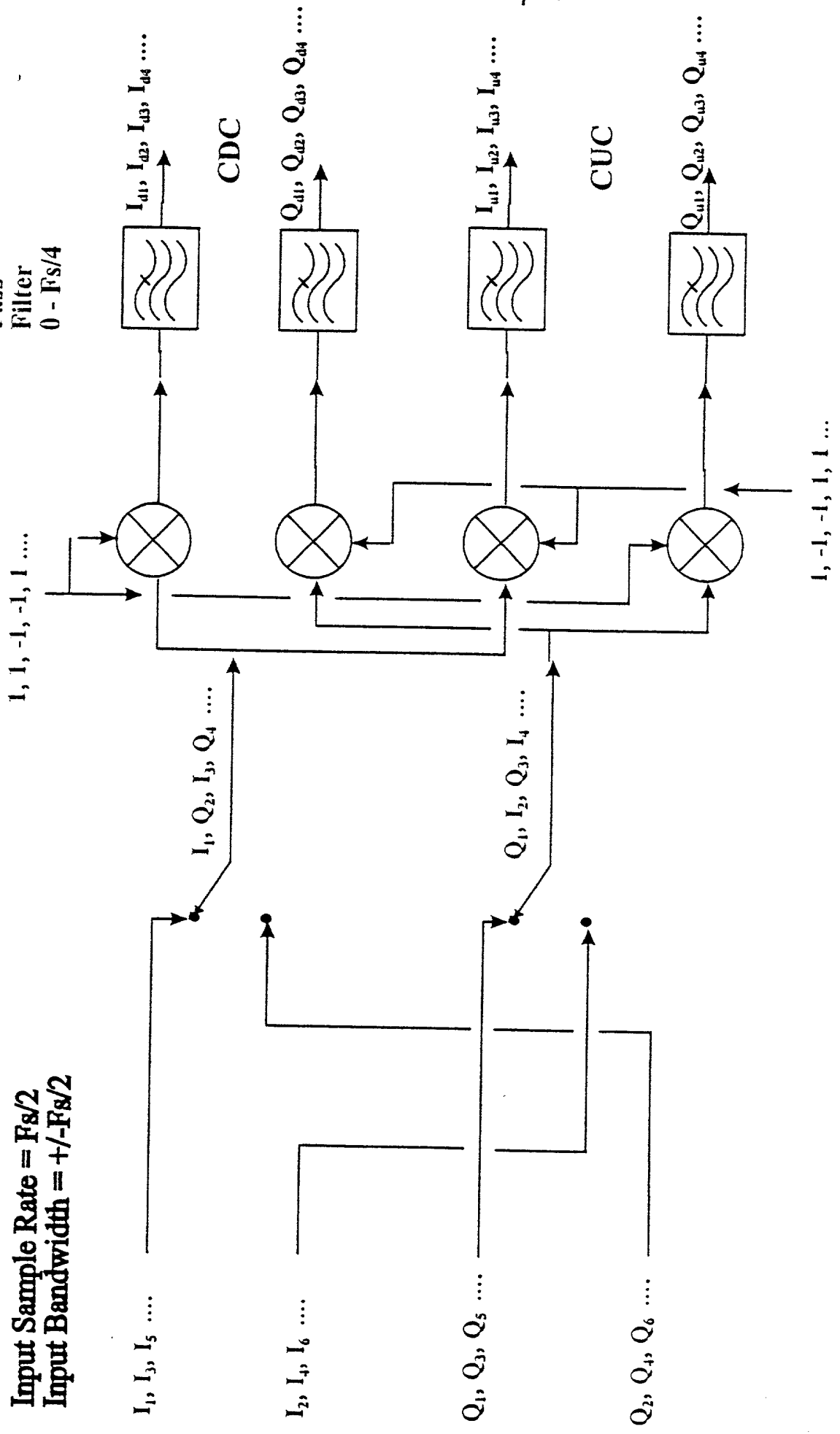


Fig. 11 COMBINED CDC(A) & CUC(A) ARCHITECTURE

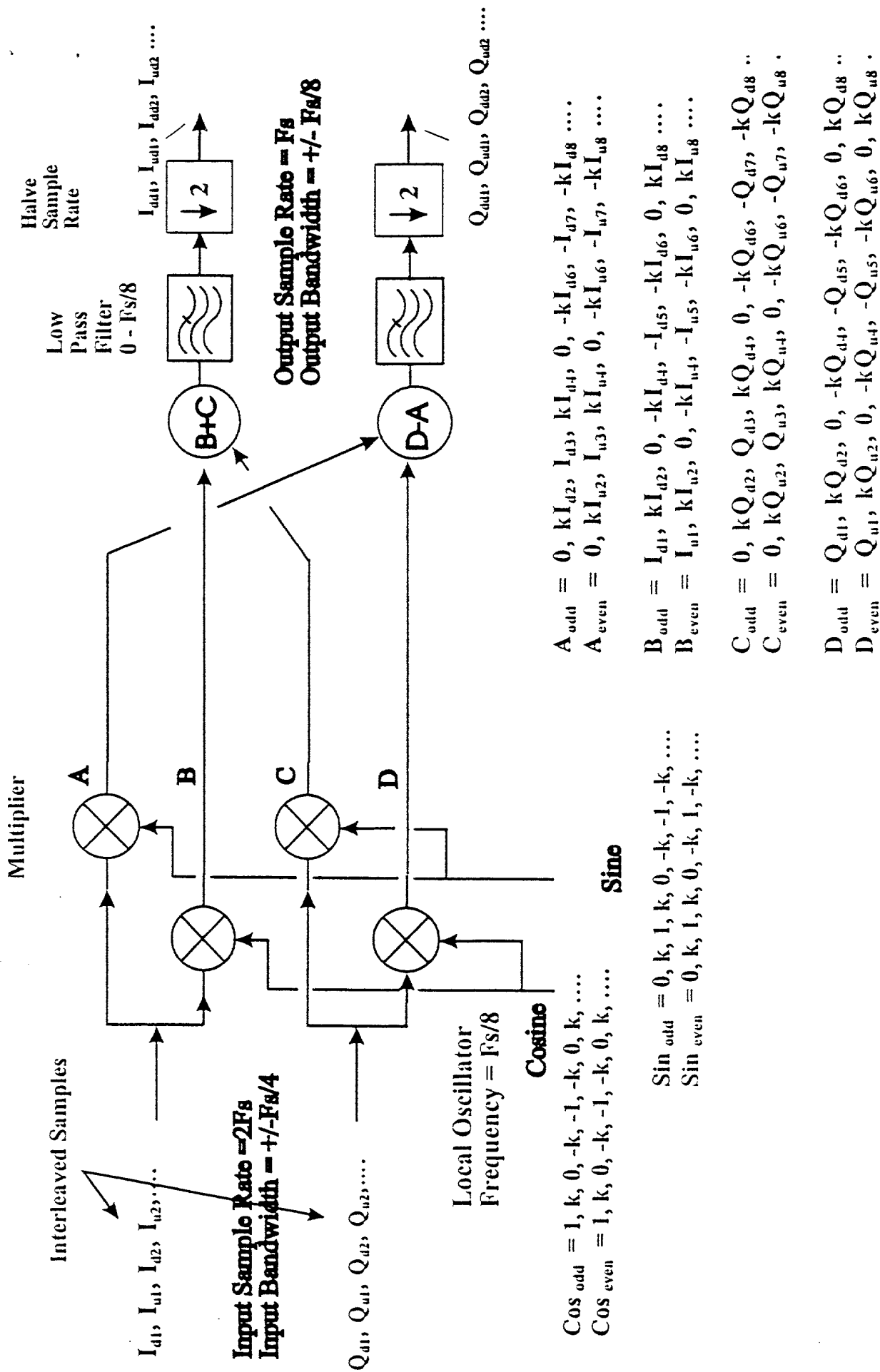


Fig. 12 BASIC ICDC(B) ARCHITECTURE

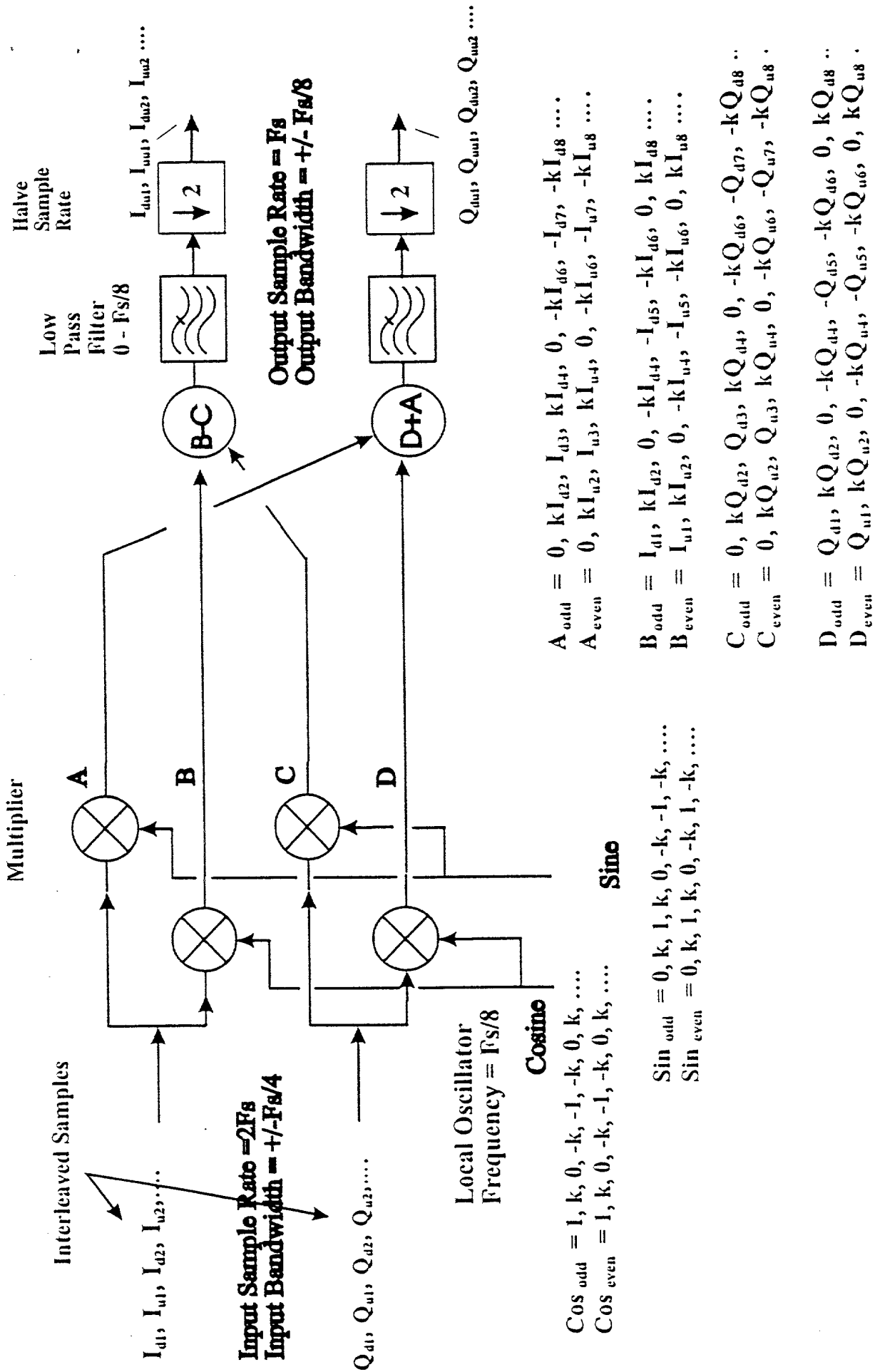


Fig. 13 BASIC ICUC(B) ARCHITECTURE

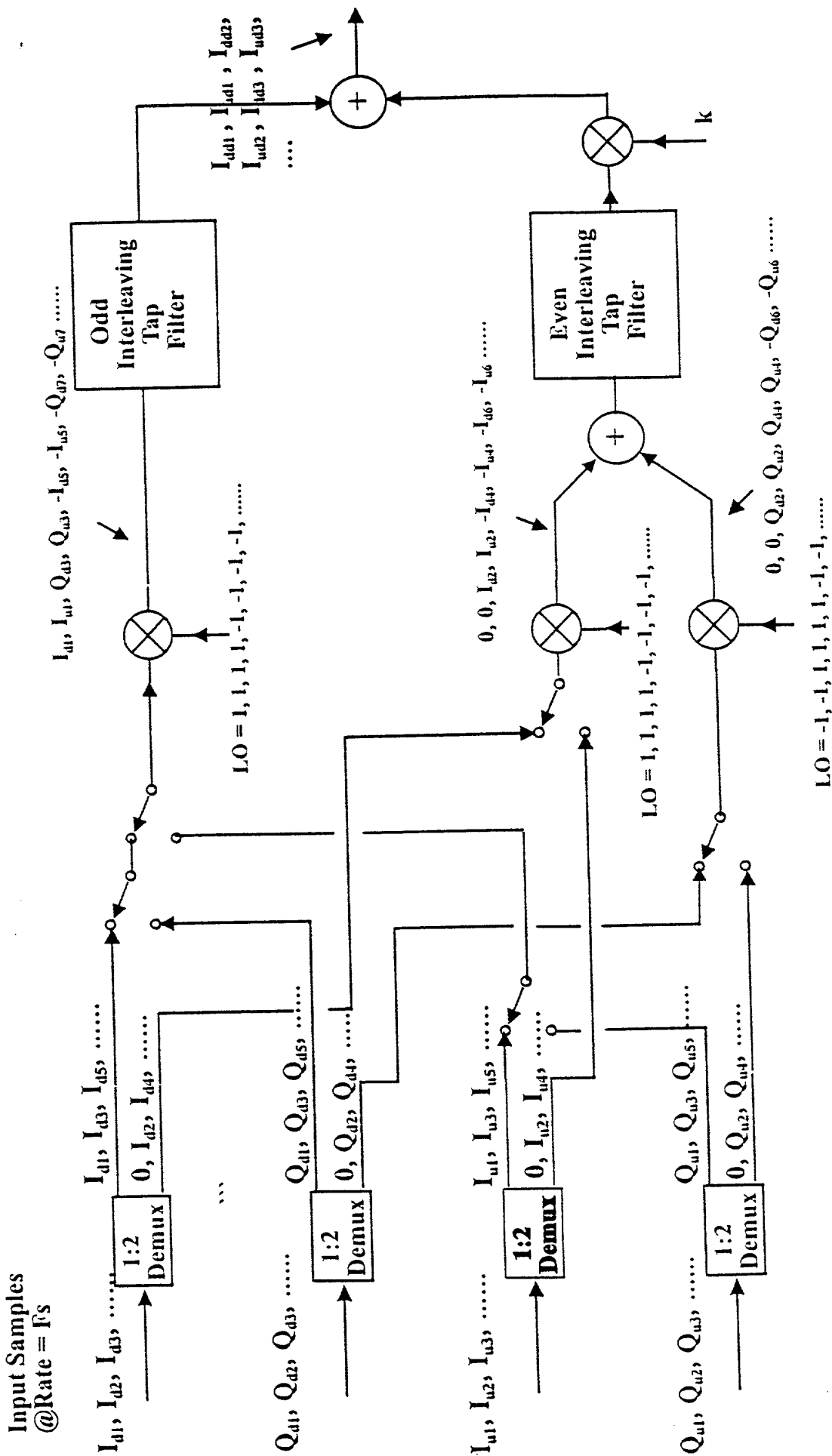


Figure 14 Simplified ICDC(B), I channel Only

Input Samples
@Rate = F_s

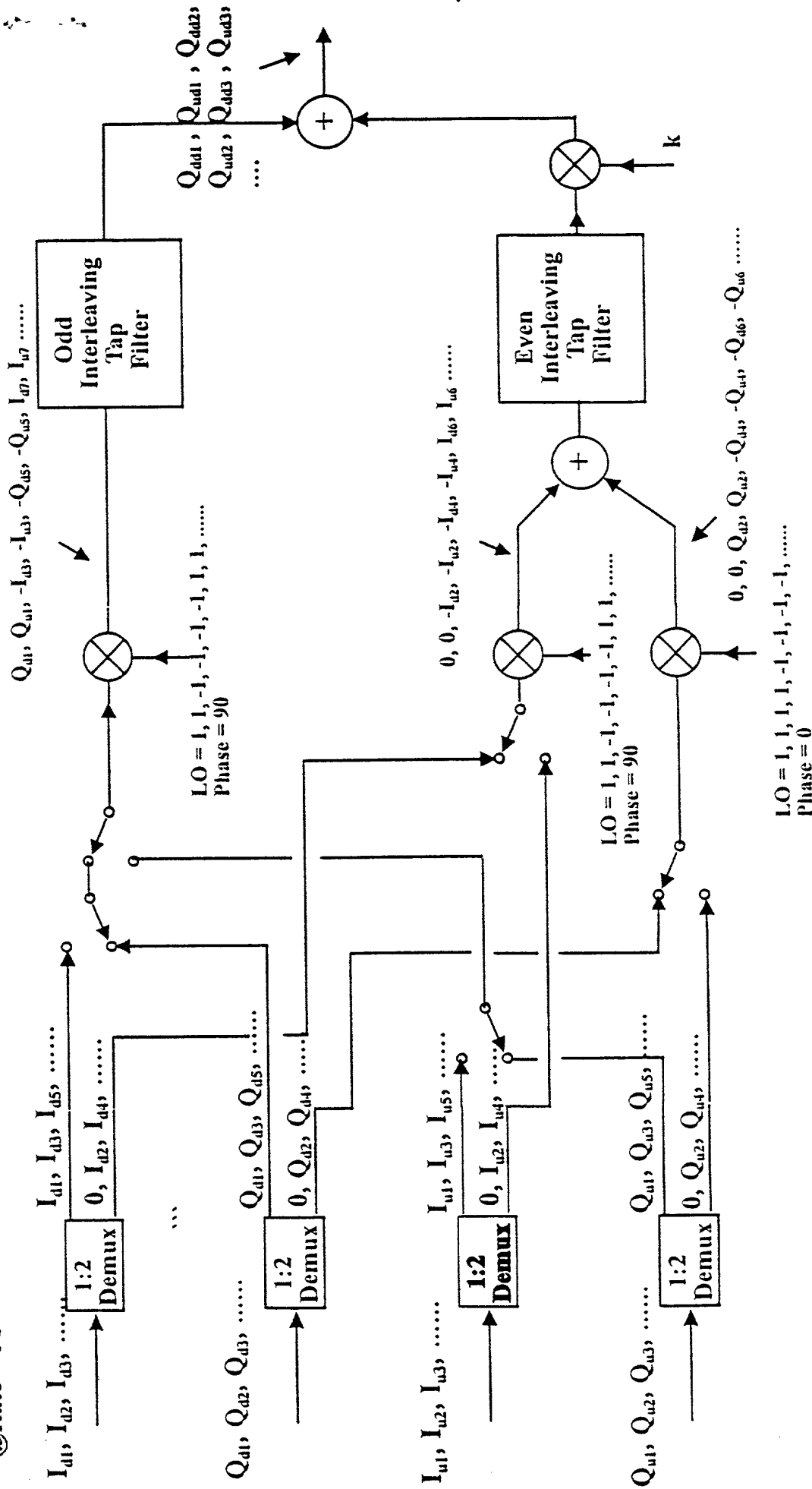


Figure 1 Simplified ICDC(B), Q channel Only

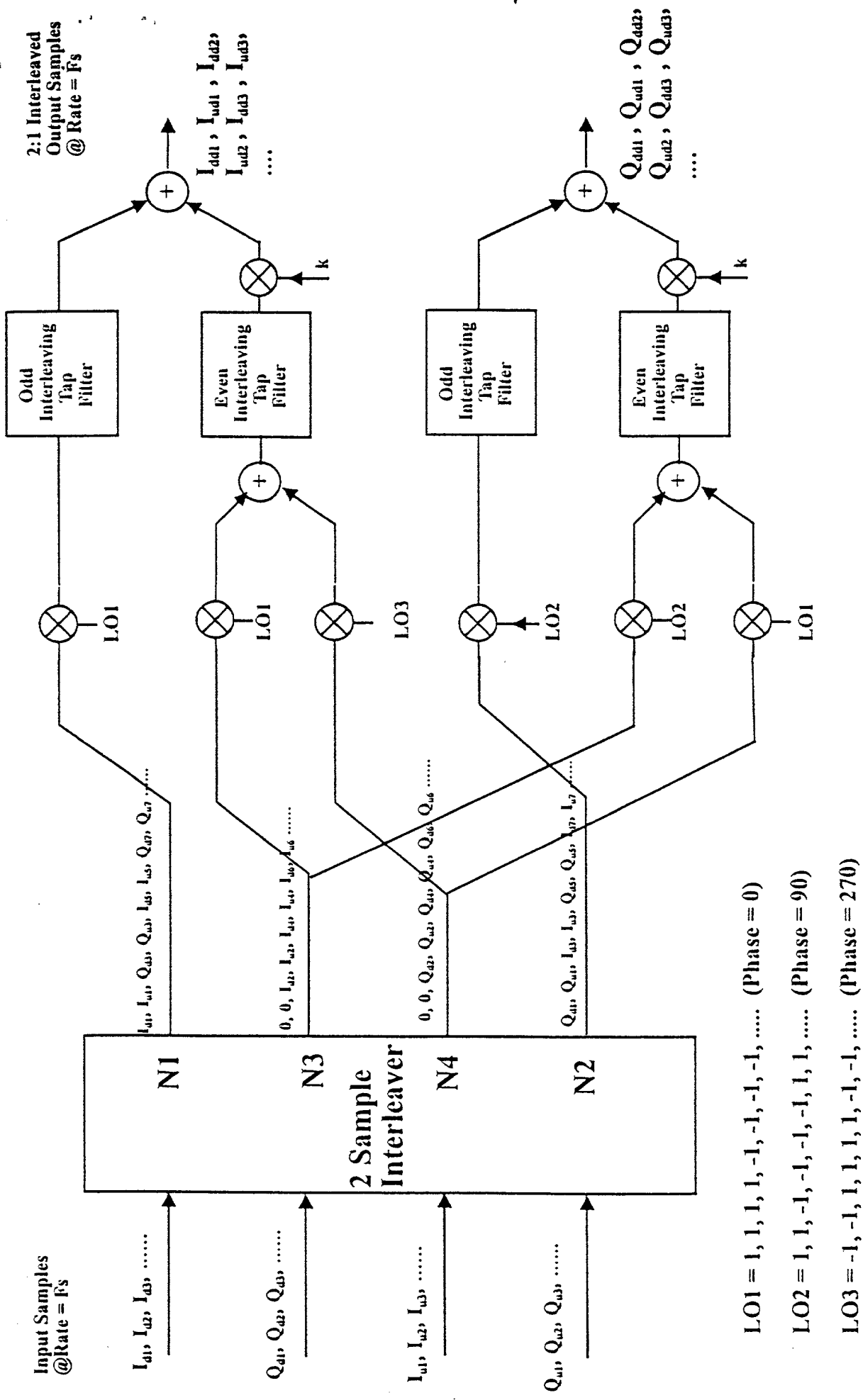


Figure 16 Simplified ICDC(B), Combined I & Q Channels

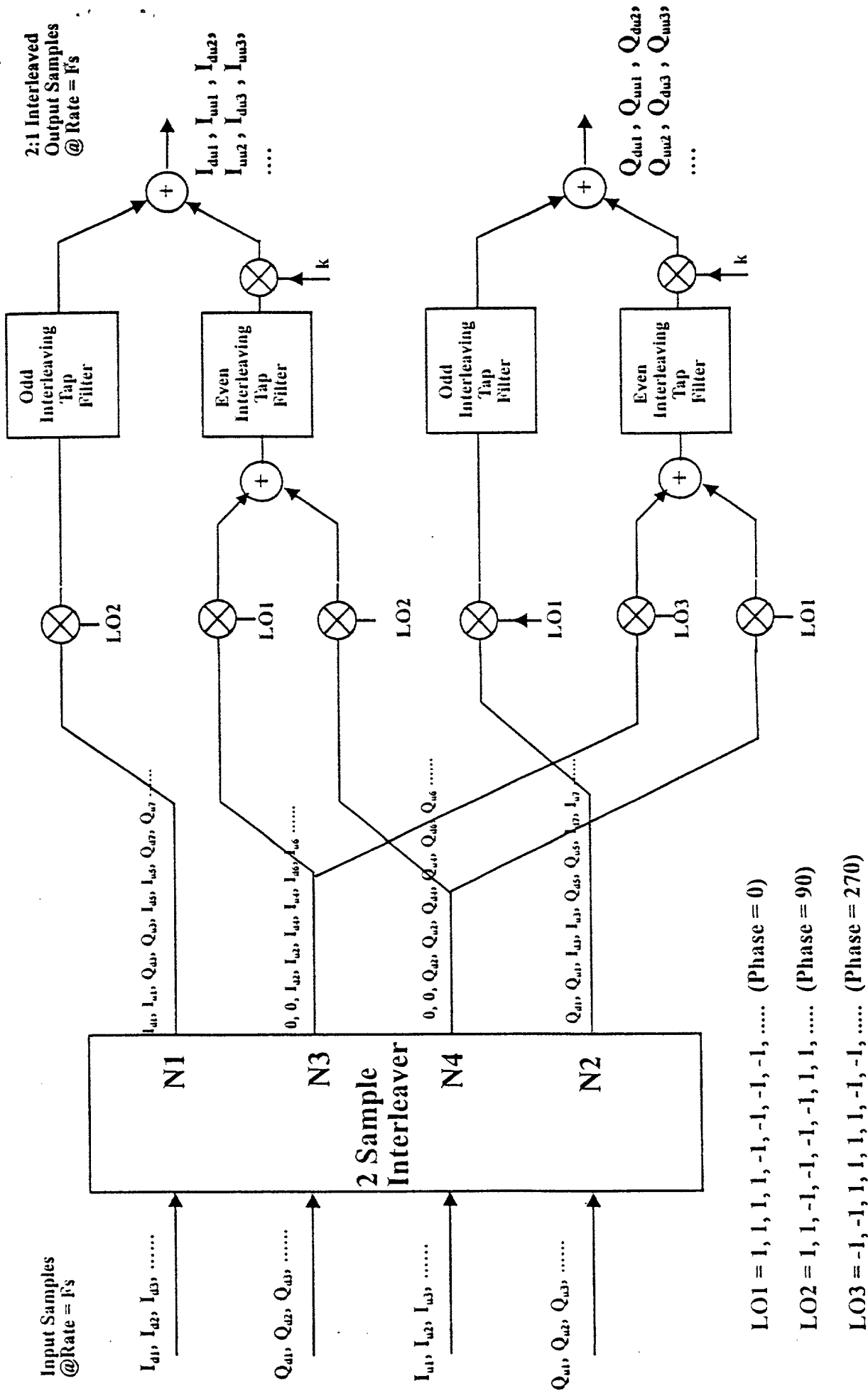


Figure 17 Simplified ICUC(B), Combined I & Q Channels

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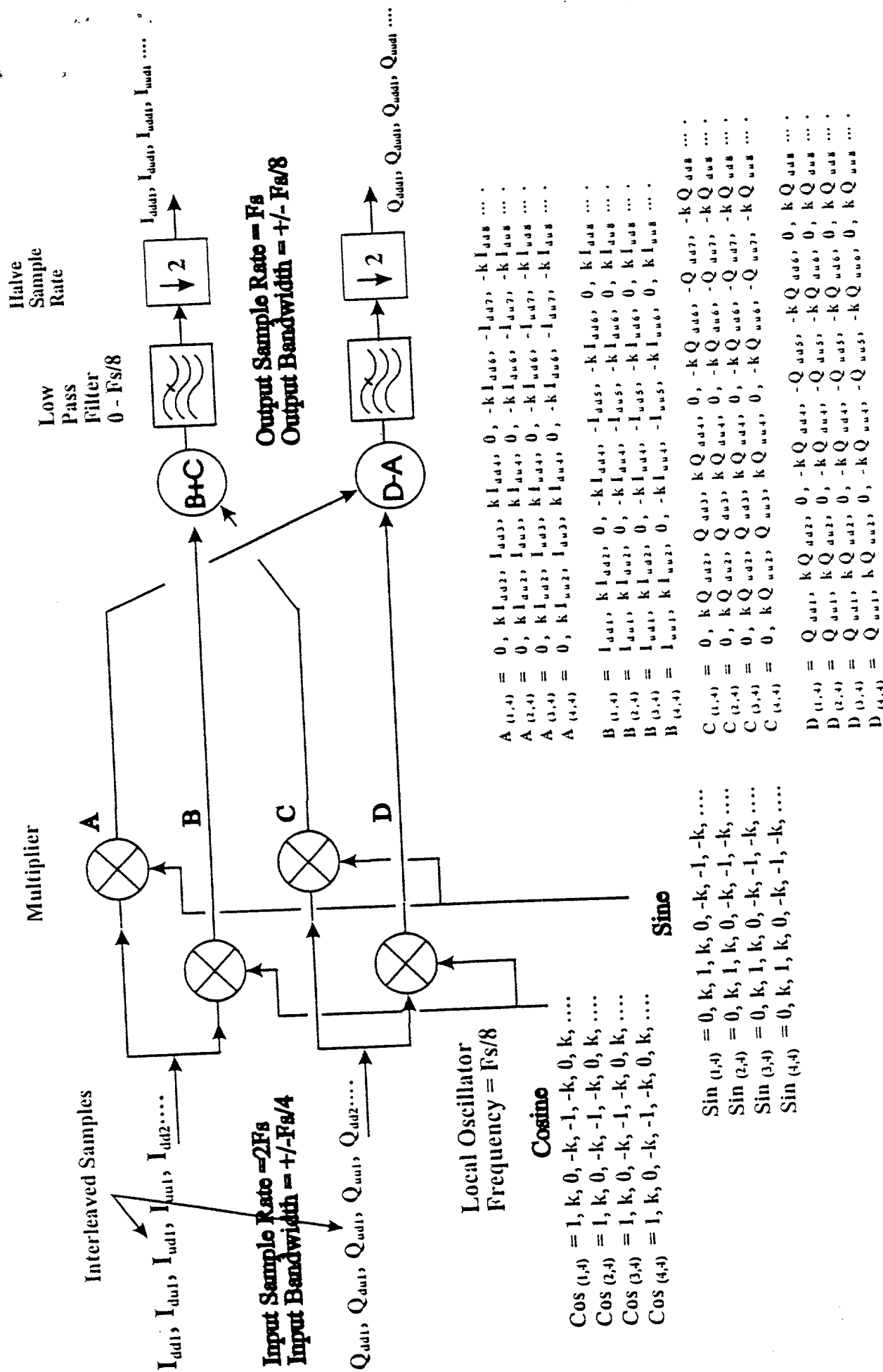


Fig. 1 & BASIC ICDC(C) ARCHITECTURE

[illegible]

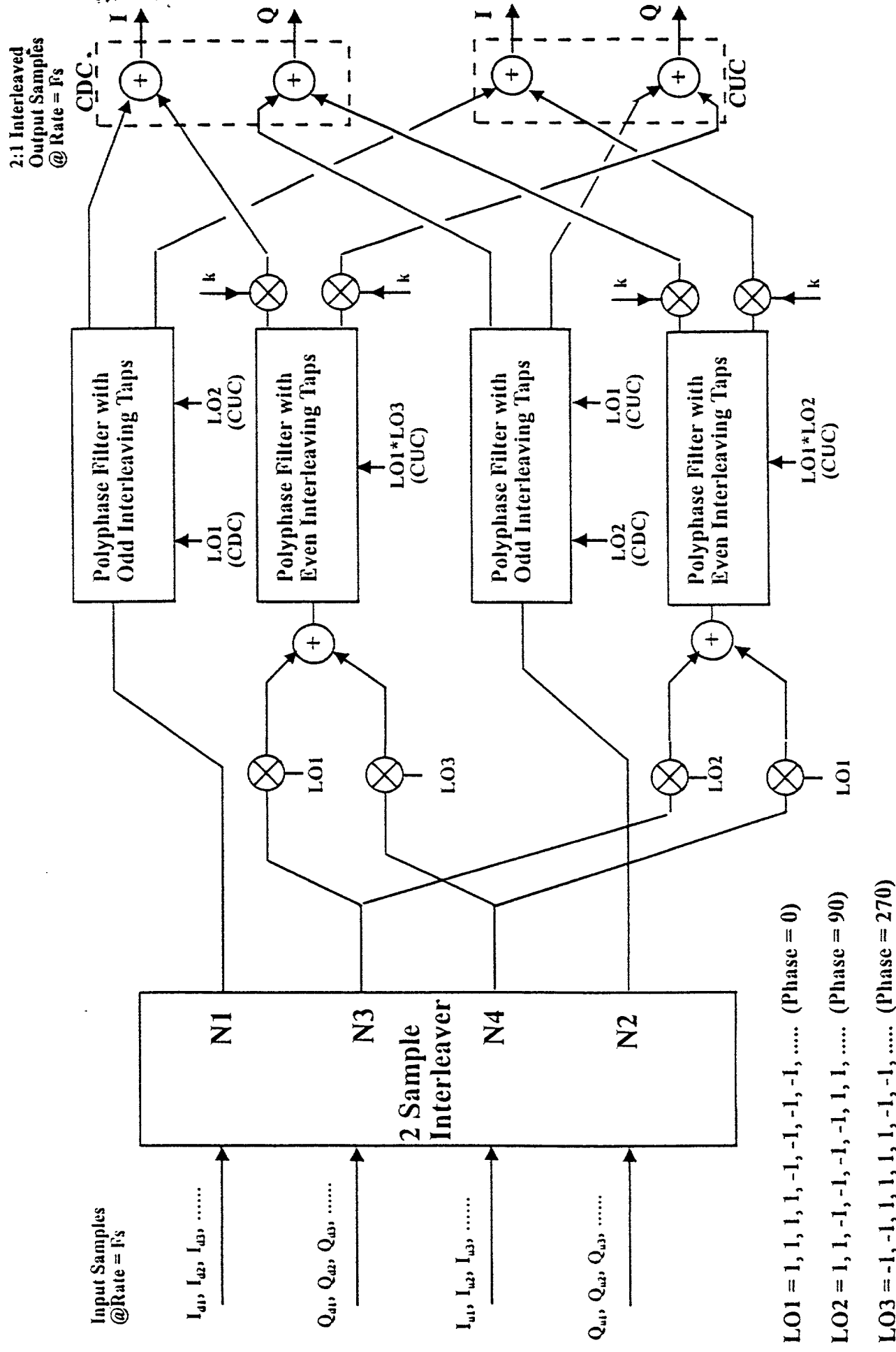


Figure 20 Combined ICDC(B) / ICUC(B) With Polyphase Filters